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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,144	03/30/2004	Tony M. Tarango	42P18570	5431

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,144	TARANGO ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☒ Claim(s) *1-7 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Office Action in response to the Amendment filed 8/17/2006.

Claims 1-19 were previously examined.

Claim 15 is cancelled.

Claims 1-14 and 16-19 are pending.

The objection to the abstract of the disclosure has been withdrawn in view of the Amendment to the Abstract.

Response to Arguments

Applicant's arguments filed with the Amendment on 8/17/2006, with respect to the rejection of claims 1-16 under 35 U.S.C. 102(e) as being anticipated by Mak et al. (US 6,885,209), have been considered but are moot in view of the new grounds of rejection, as set forth in the present Office Action.

Applicant's arguments, with respect to claims 17-19 have been fully considered and are persuasive, in view of Applicant's statement that the instant application and the Mak reference are currently owned by the same party, namely Intel Corporation. Therefore, the rejection of claims 17-19 under 35 U.S.C. 103(a) as being obvious over Mak et al. (US 6,885,209) in view of Watanabe et al. al. (US 6,522,122) has been withdrawn.

However, upon further consideration, new grounds of rejection are made as set forth in the present Office Action, below.

Claim Objections

Claims 1-7 and 17-19 are objected to because of the following informalities:

Claim 1, line 3, the comma "," between "received" and "test" should be deleted.

Claims 17 and 19, the expression "advance / retard generator" should be changed to "advance or retard generator" to indicated the proper alternative form.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Retzer (US Patent No. 5,737,369) in view of Premy (US Patent No. (6,807,498).

Regarding **independent Claims 1, 8, 11,** Retzer discloses a method for recovering data in the presence of error transients, comprising:

Disturbing a received data waveform (200, Figure 2) due to error transients introduced into the data waveform present at the Transceiver output 183 of the Receiving Terminal (140), as shown in Figures 1-4. The received waveform from the Transceiver (at 183) is routed to the Data Bit Recovery (185) corresponding to the

claimed feature of data recovery circuit DRC, which includes a conventional timing recovery circuitry (460) corresponding to the claimed feature of closed control loop, such as a phase locked loop. This timing recovery circuitry provides additional filtering to remove noise jitter in the recovered clock, and may provide additional processing, such as early/late rejection to further qualify the clock estimate. The recovered clock provides an estimate for the instant of time when the received waveform is in a stable region accurately reflecting the desired data value. The level decision (425) is sampled at this clock time (465) by sampler (430). The resulting best estimate of the recovered data is then present at the output (151), Figure 3.

Retzer does not explicitly disclose the newly added limitation, "measuring the length of time it takes the DRC to recover from the disturbance".

In analogous art, Premy (US 6,807,498) discloses a method for measuring phase locked loop (PLL) lock time, corresponding to the claimed recovery time, by deriving the PLL frequency-settling function, using signal processing block 110 for performing the lock time measurement, as illustrated in Figures 1 ad 2.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement a (PLL) lock time measurement, as taught by Premy, in the timing recovery circuitry of Retzer, since PLL lock time is a very critical parameter in applications such as cellular radios and other applications where PLL lock times are critical, it important that PLL lock times be tested in production, in order to assure ICs meet their PLL lock time specifications, using a method that would allow for measuring of PLL lock times accurately and in a short amount of time.

Regarding Claims 2-4, 9, 10, 12-14, 16, Retzer discloses introducing undesired transients at the beginning of the data waveform, causing distortion of the data waveform, which settles out over time. A sampling element (442) samples the data waveform (200), for processing by the conventional timing recovery circuitry (460), with is input to the One Bit Delay element (440), Figure 2.

Regarding Claim 5, Retzer discloses delay element 40 for delaying the received waveform by an amount equal to the period is included and a subtracting element for comparing the received waveform with the delayed waveform, and providing a timing recovery signal with zero crossing substantially less corrupted by the undesired amplitude error. A level decision (425) is sampled at this clock time (465) by sampler (430). The resulting best estimate of the recovered data is then present at the output (151), Figure 3.

Regarding Claims 6, 7, Retzer discloses a method for recovering data in the presence of error transients that includes a received waveform containing an information signal encoded at periodic time instants of a known period for eliminating an undesired amplitude error in the received waveform of a receiver. The data recovery by eliminating the undesired amplitude error can be utilized in the area of integrated circuit design validation manufacturing screening process, see Abstract.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Retzer (US Patent No. 5,737,369).

Regarding **independent Claim 17**, Retzel discloses a Receiving Terminal (140), Figure 1, comprising:

A Transceiver (180) that receives data frames from the Media (190) using Antenna (182), the Receiving Terminal (140) further comprising a Data Bit Recovery (185) which includes a sampling element (442) part of the One Bit Delay element (440) having an input 183 for receiving the data waveform (200, Figure 2) and an output 445 for sampled values. A Subtractor (450) corresponding to a generator, which receives the waveform (183) and the output 445 result from the One Bit Delay element (440), and which subtracts the output 445 from the original waveform 183, to generate output of the Subtractor (455).

With respect to claimed limitation of digital to analog converter (DAC), Retzer describes the output of the Subtractor (455) is then fed to conventional timing recovery circuitry (460), such as a phase locked loop. This timing recovery circuitry provides additional filtering to remove noise jitter in the recovered clock, and may provide additional processing, such as early/late rejection to further qualify the clock estimate. The output of the Subtractor (455) is in the analog form and therefore there is no need for the DAC, since the analog conversion is inherently performed inside the Subtractor.

Retzer does not explicitly disclose the claimed limitation of "an offset control unit with an input for a programmed test parameter".

However, Retzer describes systematic channel impairments, such as attenuation, carrier frequency offset, error transients, voltage offset, etc., which preclude fixed references and timing. Power ramping delays, or slow turn-on of the

transmitter, can distort the transmitted waveform at the begging of the transmission. Any DC offset, or overall average value offset, of the transmitted waveform will also lead to waveform distortion due to insufficient low frequency response.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to introduce an offset into the transmitted waveform as taught by Retzer, thus causing a waveform distortion for the purpose of simulating a channel impairment in order to evaluate the performance of a data recovery loop.

Regarding Claims 18, 19, According to Retzer the mixer (not shown) is part of the phase locked loop, which mixes the output of the Subtractor (455) with a reference clock to generate error correction values.

According to Retzer, the timing recovery circuitry provides additional filtering to remove noise jitter in the recovered clock, and may provide additional processing, such as early/late rejection to further qualify the clock estimate. The phase locked loop provides filtering and jitter removal on the zero crossings.

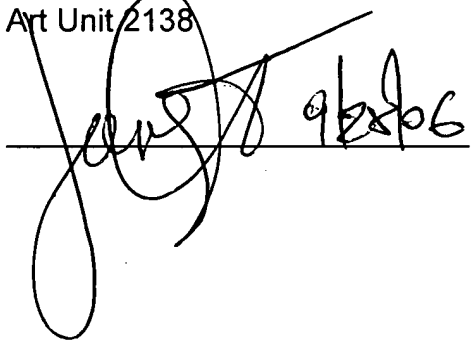
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138



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